Design of the Low Voltage Power Supply for Radio and Plasma Waves Investigation Instrument and ESA/JUICE Mission

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Abstract

European Space Agency's selected Large-class mission called JUICE to study Jupiter and its icy moons environment will carry the Radio and Plasma Waves Investigation instrument aboard during more than 11 years long mission. It will characterize incident radio waves, perform multipoint in-situ plasma impedance measurements, carry triplet of search coil magnetometers and perform data preprocessing. Low Voltage Power Supply unit hereby presented have to deliver very low noisy stabilized power to sensitive instruments working from DC up to 45 MHz, distribute low jitter synchronization clock to respective subunits and provide with housekeeping telemetry measurements. It was designed to meet or exceed Total Ionizing Dose requirement of at least 50 kRad(Si).

Keywords: ESA JUICE, RPWI, low voltage power supply, radiation, space

1. Introduction

Swedish Institute of Space Physics in Uppsala (IRFU) has been selected as one of ten leading institutes responsible for delivery of scientific instruments to be flown on European Space Agency's first ever mission to Jupiter to perform in-situ study of its radio emissions and plasma environment. Jupiter Icy Moon Explorer (JUICE) [1] is also by far one of the most challenging agency's mission. Among various optical instruments such as cameras or laser altimeter, one of the scientific goals is to detect sub-surface currents induced by flowing oceans underneath the crust of Ganymede or Europa moons using only ultra sensitive fluxgate magnetometer. Astronomical Institute of the Czech Academy of Sciences (AsU) has been asked to develop ultra low noise and reliable cold redundant Low Voltage Power Supply unit.

Key design drivers were mainly determined by the mission operational environment with highly energetic trapped particles and cosmic radiation together with conservative component selection approach required by ESA Product Assurance and Risk Management strategy. The instrument allocated long term average power is limited to 14.7 W only.

2. System Package Overview

The Radio and Plasma Waves Investigation (RPWI) instrument sensor set consist of orthogonal triplet of 2.5 meter long monopole antennas of the Radio Wave Instrument (RWI) for RF vector measurements, medium frequency 3-axis Search Coil Magnetometer (SCM) and four Langmuir Probes and Plasma Waves Investigation (LP-PWI) setup to map mutual impedances of the local plasma environment. Mission goals of the satellite equipped with 90 m^2 of MPPT-regulated solar panels also impose very strict Electromagnetic Compatibility requirements on all payloads.

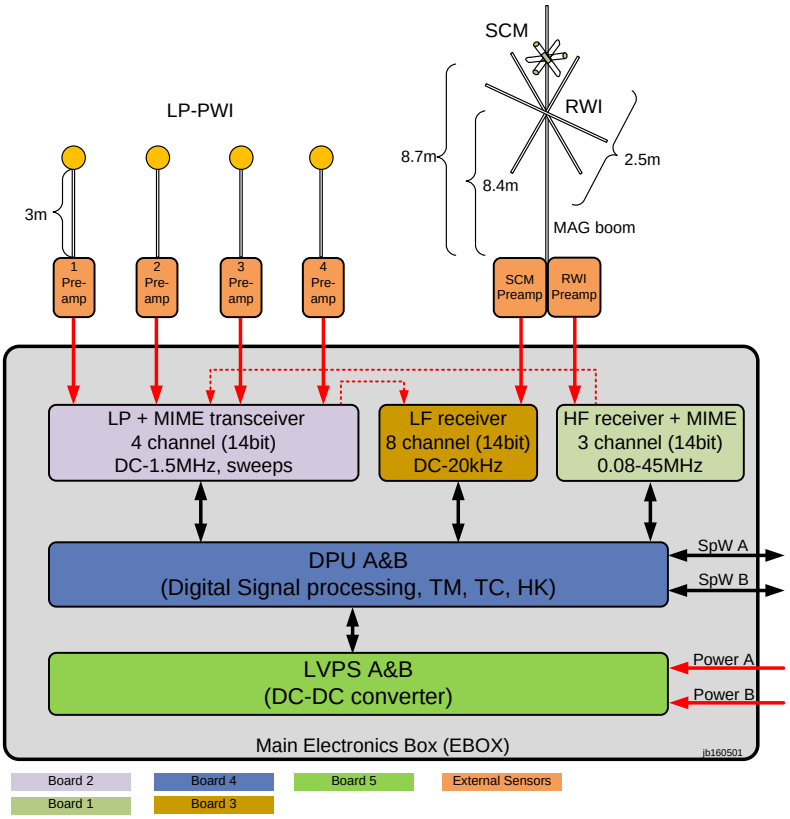

Figure 1: Radio and Plasma Waves Investigation (RPWI) instrument block diagram.

A total of three analyzers plus two cold redundant data processing units (DPU) are encapsulated within the common Electronic Box (EBOX). They are: High Frequency analyzer (HF), Langmuir Probe - Mutual Impedance Measurement Equipment (LP-MIME) and Low Frequency analyzer (LF). Respective subunits within the RPWI instrument and their interconnection are described in the block diagram in Figure 1. LVPS part is divided into two cold redundant units marked as A and B.

3. LVPS Unit Requirements

The most important LVPS requirements defined by the JUICE/RPWI Experiment Interface Document (EID-B) are summarized in the Table 1.

Table 1 : LVPS Unit Requirements

Requirement	Value
Input Voltage Range	26-31 V, with ±1V UVLO hysteresis
Output Power	10.7 W long term average, 20.3 W peak
Output Voltages	3.7V ± 5% @ 3.9A, +9.75V ± 10% @ 0.35A, -9.75V ± 10% @ 0.25A (peak), 10 different outputs: 8 controlled, 2 fixed
Switching Frequency	125 kHz or 250, 375, 500 up to 1 MHz

Noise	Output differential mode noise less than 4 mV_{ppRMS}, common mode conducted emissions on input less than 40 dBμA in DC-50 MHz region
Output Clock + Internal Synchronization	50 MHz LVDS star-distributed clock output to each instrument, synchronized converter switching clock
Galvanic Insulation	Primary to secondary ground (to chassis) more than 1 MΩ, less than 150 nF
Dynamic Range of Control Loop	Minimum Load of 3.7V @ 0.1A, 50° or better phase margin, 10 dB or better gain margin for unit End-of-Life
Data Interface	telemetry and telecommand via LVCMOS 115200-8-N-1 bus
Efficiency	75% or better at average power output
Mass	Less than 400 g, including connectors, conformal coating, excluding mechanical frame and mounting accessories
Redundancy	Fully cold redundant design with power distribution circuitry
Radiation Tolerance	TID 50 kRad(Si) or better
Protections	UVLO, OVC, OVL, OVP on primary converter side OVP on each voltage level of the secondary side OVC, slow start on each output of the secondary side

The summary identifies that for the in-situ radio measurements the common switch mode power supply and power electronics frequency plan shall be based on 125 kHz and its (sub)harmonics. As the RPWI instrument work with capturing and preprocessing electromagnetic spectra using high speed precision analog to digital converters (ADC), the main system design approach is to keep control over the self generated noise. Harmonics of local disturbances shall be deterministic to be able to be subtracted from scientific data afterwards. Moreover, there are several point-of-load (PoL) switch mode power converters for low voltage / high current digital circuits distributed over dedicated boards. The RPWI topology uses the synchronization clock signal provided by the LVPS unit referenced to power supply secondary ground connected to chassis. DPU subsystem requires 50 MHz LVDS clock to feed the SpaceWire [5] interface required for communication with spacecraft. Subunits derive synchronization clock signals by respective dividers locally using field programmable gate arrays (FPGA). A direct connection of the DPU to the LVPS output assures the minimum load conditions and continuous mode of the converter.

4. Design Considerations & Topology Selection

One of the major design decision made based on very critical power conversion efficiency demand was to not implement conventional 12V MOSFET drivers and PWM controllers such as UC1825 and its clones. Moreover, this commonly used family of single chip PWM controllers is marketed as radiation tolerant with around 30-50 kRad(Si) total ionizing dose (TID) tolerance only, mostly dedicated for LEO markets with sufficient radiation shielding mass and available power.

Table 2 : Converter Topologies for the LVPS design

Topology	**Pros +**	**Cons -**
Flyback	• very simple driving design • 1 MOSFET switch only • simplicity • no optical feedback needed • low components count	• only rad tolerant 30-50 kRad(Si) PWM ICs for LEO and MEO available • single output rectifier have to handle currents up to 6-8 Amps in average, two times more per component than with push-pull topology • high current Schottky diodes have high capacitance and

		high reverse leakage at high temperature, decreasing converter efficiency • low bandwidth, worse step response • high noise level, higher conducted and radiated emissions • transformer core utilization only with max. 50% of B-H curve, bulky and EMI shielded transformer needed
Push-Pull Forward Converter	• distributes power dissipation stress into two power switches and two Schottky diodes in output rectifier	• not available rad hard PWM controller for low voltage (digital MOSFETs) operations • only rad tolerant drivers available 30-50 kRad(Si) • transformer is not driven with balanced and fixed duty cycle, B-H curve is not utilized optimally leading to lower efficiency
Integrated (IC Driver) Cascaded Current-Fed Push-Pull Converter [2]	• compact converter footprint • Buck inductor acts as output filter reducing need for bulky output LC pairs	• not available rad hard PWM controller • current feedback controller IC input signal might be sensitive to noise/SEEs • precise PCB layout and control signals routing for feedback signal needed (current feedback control) • under radiation conditions missing pulses behavior have to be investigated on driver IC case-by-case • driving signals of both Buck and push-pull MOSFET switches needs overlap to keep constant current conduction
Integrated (IC Driver) Cascaded Voltage-Fed Push-Pull Converter	• compact converter footprint Voltage feedback less sensitive to noise / SEE or quality of PCB signals routing wrt. current mode control	• not available rad hard PWM controller for low voltage operations
S.M.A.R.T. (Standard Multiple Application Regulator Topology) Converter [3] / Discrete Current Fed Push-Pull Converter	• ESA flight-proven • scalable design, documented, tested • discrete design based on ITAR-Free components	• current-fed push-pull driving may run into short circuit current due to the overlap in P-P stage driver clock timing at higher radiation doses • auxiliary winding for feedback may become problem with push-pull driving imbalance • design is not efficiency-optimized • slow feedback loop (~2.4 kHz in [3]) • unstable RC oscillator clocking • based on CMOS logic family
Discrete Cascaded Voltage-Fed Push-Pull DC-DC Converter	• combines pros of push-pull topology (optimized transformer core utilization with 100% of B-H curve, smaller core wrt. flyback) • no feedback form secondary side required • radiation Tolerance defined by respective components, scalable up to hundreds of kRads with conventional logic and analog IC • each converter design parameter (timing, slow start, inrush limiting, driving capabilities) are fully scalable • very fast switching operations up to 500 / 250 kHz • stable feedback bandwidth up to 1/20 - 1/10 th of buck stage switching frequency	• discrete design with slightly higher complexity

The only viable controller for deep space and harsh environment missions radiation hardened up to the level of 1 MRad(Si) at a time of the design phase was the PWM controller with push-pull driving capability and 5 V power supply voltage only PWM5032/PWM5031 by Aeroflex/COBHAM. As the US export controlled product with radiation tolerance more than 500 kRad(Si) it belongs under United States Munitions List and is thus covered by International Traffic in Arms Regulation (ITAR). To shorten the time necessary to complete the paperwork during the early design phase of any critical part in the design this controller was rejected. With finally decided discrete-based solution, whole Engineering Model is completely based on very low cost and easily available COTS replacements and thus ITAR/USML parts free making the development much faster and cheaper.

From the LVPS unit requirements, reliability, component count and price point of view there were only following topologies for the design considerations identified and summarized in table 2. Parameters mentioned in the summary table are tailored to 10-20 W class power converters with respect to LVPS unit requirements. They do not reflect high power ratings in order of kilowatts such as described within topology pros and cons discussion in [4]. Hereby mentioned comparison has to be understood as with respect to the RPWI LVPS case. Finally, the discrete-based cascaded voltage-fed push-pull DC-DC converter topology was selected for the implementation.

5. Principle of Operations

The block diagram of identical main and redundant LVPS units is given in Figure 3. The buck pre-converter on primary side was selected as a fixed voltage source for the following push-pull transformer to achieve multiple output levels. Fixed push-pull stage duty cycle is beneficial mainly to equalize power dissipation between driving transistors and output rectifiers and transformer magnetization periodical resets. It was originally assumed for the implementation of synchronous rectification (SR) with fixed gate drive timing as very convenient for floating gate drive of SR switches. Single stage push-pull forward topology with variable duty cycle of each primary switch might not optimally drive secondary side SR switches.

As the SR is beneficial only when a sum of driving and conduction losses is lower than conduction losses of Schottky diodes during long-time period of nominal output power load with respect to idle load, the total efficiency impact was not taken into account and the whole SR circuitry was finally removed to decrease the complexity of output rectification circuits, hence also the cost.

The buck stage power switch has been changed from proposed [3] P-MOSFET type to the N-type with lower R_{DSon}. It is controlled by associated gate drive transformer (GDT). Floating gate drive allows converter to operate with much wider input voltage range with respect to original converter [3] where resistor-based level shifter was used. In the similar stage mentioned in design [3] continual power losses in order of 0.5-1.5 W were shunt-dissipated via resistor divider network.

The converter control and driving circuits associated with primary side ground potential are based on 5 V level logic circuits, including push-pull driver and buck switch to conform with AC-logic family. As sawtooth generator simple BJT switch and RC link is utilized. Dedicated fast rad hard rail-to-rail op-amp is used as error amplifier in conjunction with discrete comparator as a PWM modulator.

After power up, the RC oscillator tuned to frequency close to 250 kHz boots up and drives the converter. Once the secondary 3.7 V rail output further LDO-stabilized to 3.3 V is fully charged, the crystal oscillator starts to feed the FPGA with 50 MHz clock. Digital core provides additional 200 ms delay line as a safety margin to distribute divided clock signal of 250 kHz back to the primary side once the converter is fully charged and ready for synchronization clock takeover. The same type of the 1:2 ratio GDT utilized in buck floating driver stage performs the galvanic insulation for backward clock transfer. Whilst the step down converter works at 250 kHz, the push-pull transformer is driven by 125 kHz signal coming from the D-type divider to utilize the pre-converter symmetrically. A successful test run on double switching frequency of 500 / 250 kHz was also performed to proof the scalability of proposed topology with aim to further decrease the filter inductors in future designs. Once the timing circuitry connected with primary side ground potential recognizes new switching signal coming out of the secondary side FPGA feed, it takes over the synchronized clock, whilst stops the RC oscillator to reduce the power consumption. Converter is then fully synchronized to 50 MHz clock distributed to all other RPWI subsystems and easily recognizable within the EMC spectra. The clock synchronization takeover event is captured in Figure 2.

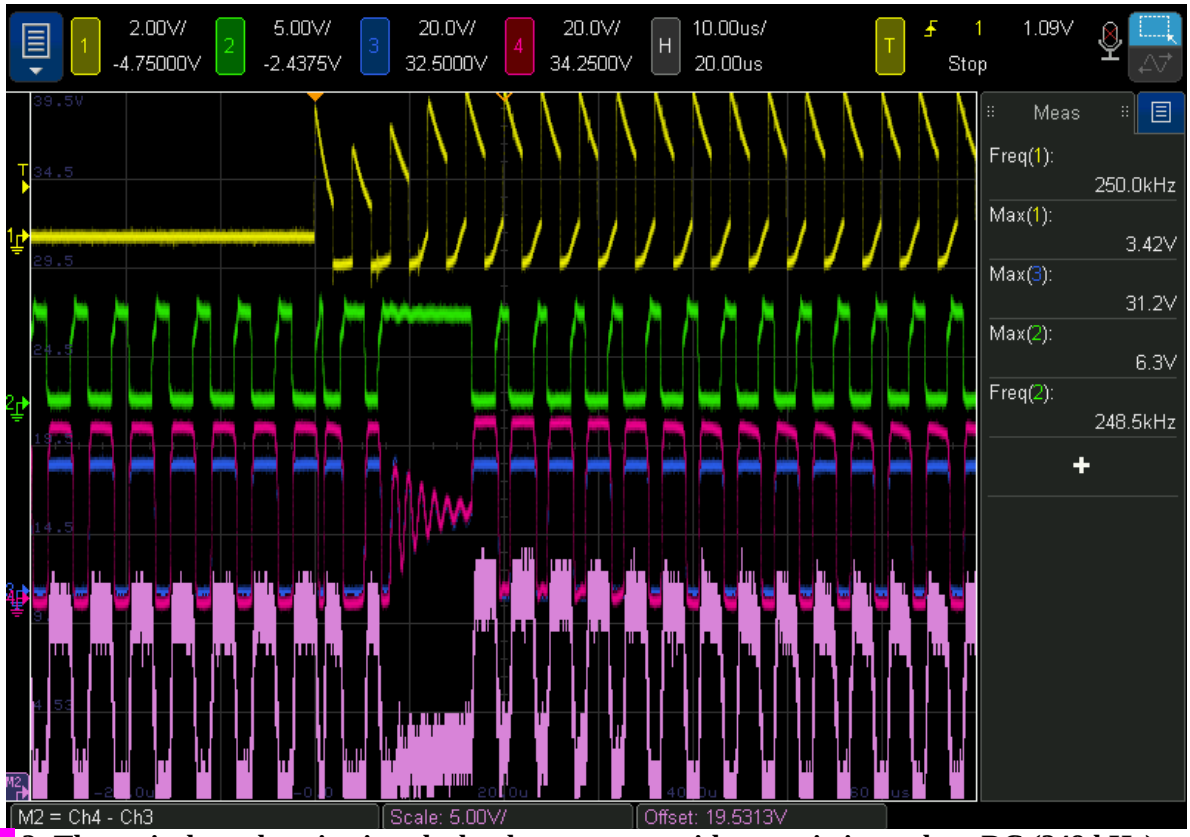

Figure 2: The typical synchronization clock takeover event with two missing pulses. RC (248 kHz) and XO (250 kHz) controlled clock. From top to bottom: Recovered FPGA clock signal referenced to primary ground potential, buck MOSFET driving signal, buck MOSFET Gate + Source potential, buck MOSFET V_{GS} driving signal waveform.

FPGA state machine then enters the mode where awaits the reception of TM/TC requests to turn On and Off respective subunit rails or to reply data grams with housekeeping measurements.

6. Voltage Feedback Regulation

On JUICE mission, no optocouplers conventionally employed in PWM controller feedback loops are wise to be used unless special radiation testing or bulky spot-shielding is included. The radiation environment may degrade strongly their current transfer ratio (CTR) parameter and disable long term operations of the whole converter.
Up to the time of the release of this paper also no magnetically-coupled voltage feedback amplifiers or drivers with sufficient gain, phase margin and bandwidth in radiation hardened version were available. The feedback controller UC1901-SP utilized in similar power supply unit solutions for ESA Solar Orbiter mission was concluded to be not fully characterized as suitable for JUICE operational environment. Auxiliary winding voltage feedback does not work properly there, as the possible imbalance in push-pull transistors, possible missing pulses and varying transformer impedance could strongly affect the feedback loop parameters and voltage output variations. The feedback regulation scheme is considered as a converter with minimized output impedance (voltage source) and only the buck converter feeding the push-pull forward converter stage is voltage-controlled. The total output impedance on 3.7 V bus is in order of 50 mΩ (referenced to secondary ground) which fits the technical requirements for various load conditions well. The advantage of low impedance assumption is the voltage feedback loop referenced to primary ground with no DC coupled feedback from the secondary side grounding. Primary side of the converter is DC floating with respect to LVPS unit chassis to prevent grounding loops with main spacecraft power supply. Beginning of Life (BoL) gain margin of 20 dB, phase margin of 70°, and 10 kHz bandwidth were measured as minimum values over the whole range of load conditions.

7. Circuit Protections

The LVPS implements following list of safety features:

- Under Voltage Lockout (UVLO) with hysteresis (25 ± 1V) independent on input voltage rise time from 0 to operational 28V to ensure proper circuits biasing at converter startup
- Overvoltage Protection (OVP) on buck stage node blocking the push-pull stage drivers using AND logic to prevent output capacitors to exceeds rated voltages
- Overload protection (OVL) on push-pull stage with two reaction time modes (fast + slow)
- digitally controlled output current thresholds on all rails utilizing FPGA softcore
- digitally controlled output voltages on all three voltage levels as secondary OVP
- analog current limiter circuits on each output rail

There are two timing modes of protections implemented on primary side. Fast reacting protection mode is based on cycle-by-cycle control principle utilizing push-pull current sensing. Wide bandwidth (~1 MHz) BJT-based circuit is used for push-pull driver gating. Slow mode protection activates thyristor-based memory latching circuit in case of long lasting anomaly (order of ms) to prevent sudden influence of in-flight SEE events (10-100 μs). If the protection latches, the LVPS have to be power cycled to restart with at least 5 seconds for internal capacitors discharge. The FPGA softcore task is to continuously process the current and voltage values readout from associated ADCs and compares them with preset values. Once three consecutive samples exceeds the limit, the respective output rail switch is turned off via dedicated control signal pin. Averaging of three values is implemented to exclude non-destructive SEE events or fast current spikes transients from undesired turn off decision. Once the limit is reached, the output is turned off in less than 3 ms. All preset values are stored in FPGA RAM registers and configurable throughout the mission lifetime via telecommand. Implicit values are burned into the ROM memory for startup settings.

8. Flight Model Component Selection

All critical components selected for the Flight Model units were picked up based on their fully electrical equivalents availability on COTS market. All semiconductor components summarized in Table 3 are available in rad hard versions with at least 100 kRad(Si) HDR and 50 kRad(Si) ELDRS TID levels. Their high level grade requires complying with US export control. However, it still does not contain any ITAR/USML parts.

Table 3 : Critical EEE parts selection summary

Category	Part Designator
Main Transformer	EFD-25 with 20 pin extension headers
Pulse Transformer	GDT91 M90
CM, DM Inductors	CMC15 1M0, SESI 15 M10, SESI 15 6K4, SESI 9.1 33K
LDO	RHFL4913A-ADJ
Analog comparator	LM193QML-SP
R-R Op-amp	RH1498
Quad I/V converter	MSK496
N-MOSFET	IRHLNJ77034, IRHNJ57Z30, IRHNJ57130
P-MOSFET	IRHNJ597Z30, IRHMS597Z60
Schottky diodes	1N5819UR-1, 30SCLJQ030, 1N5811US, 1N5822US
Crystal oscillator	VECTRON 1220, 50 MHz
LVDS	RHFLVDS31AK1
Logic family	54AC00, 54AC08, 54AC74
A/D converter	ADC128S102QML
FPGA	RTSX72SU-CQ208E

9. Test Results

Unit performance under minimum and maximum load conditions was tested using the Engineering Model units in Figure 4. Ambient temperature conditions were applied initially during the tests procedure. Later on the thermal test in the range of -30 to +80°C confirmed the functionality. To prevent ice growth and potential influence to uncoated electrical circuits around freezing and melting point the flow of nitrogen was injected into the non-vacuum thermal chamber in Figure 5.

Exceptionally good conducted emissions (CE) test results in Figure 7 and Figure 8 with differential and single ended modes respectively met and exceeded unit requirements. The output differential conducted emissions test result is given in Figure 9. Measured peak converter efficiency was determined as 78.2% at 28 V and full load conditions, excluding losses on output power switches. With power distribution unit MOSFET switches included the total efficiency fall to 72 %. Dummy load unit, measurement principle and associated harness with excessive length are contributing strongly to the efficiency decrease. Further investigation is planned for potential setup optimization, Flight Model units manufacturing and delivery. Thermal camera snapshot of the fully loaded converter under free convection air cooling not exceeding 40°C is illustrated in Figure 10.

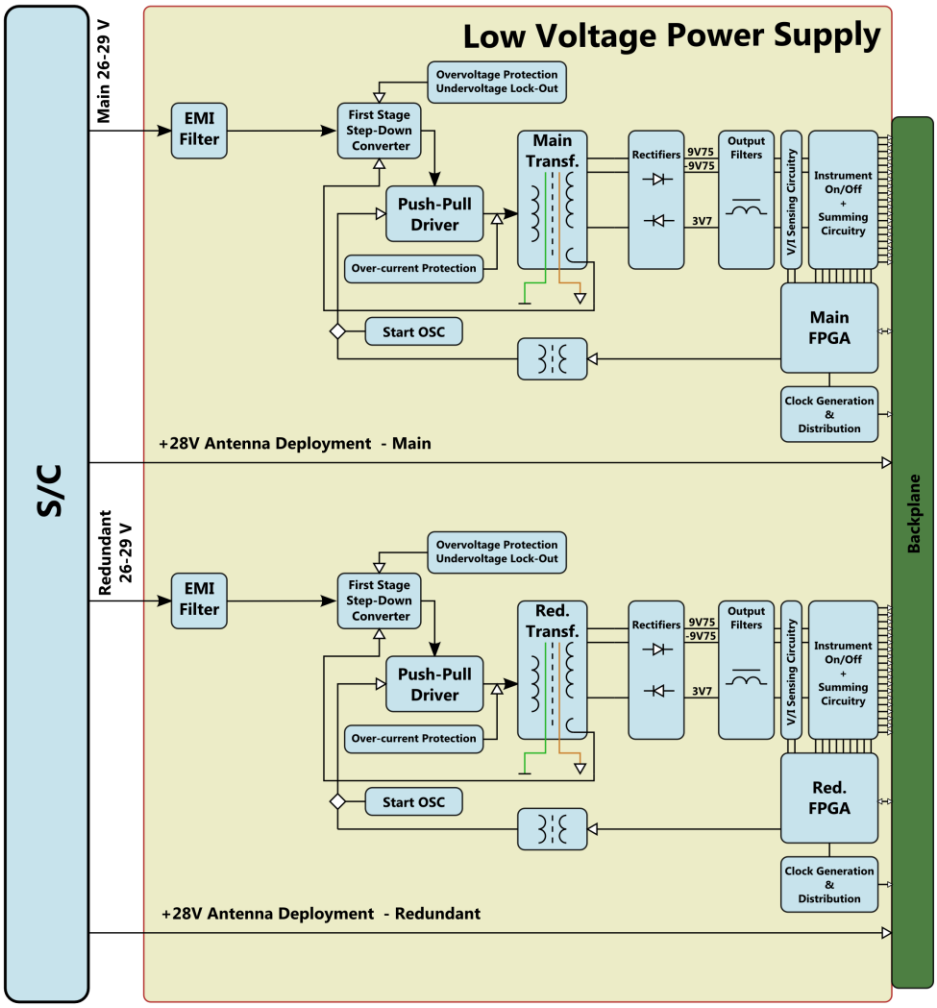

Figure 3: RPWI Low Voltage Power Supply Block Diagram. Two Cold-redundant units are connected to all subsystems via backplane board.

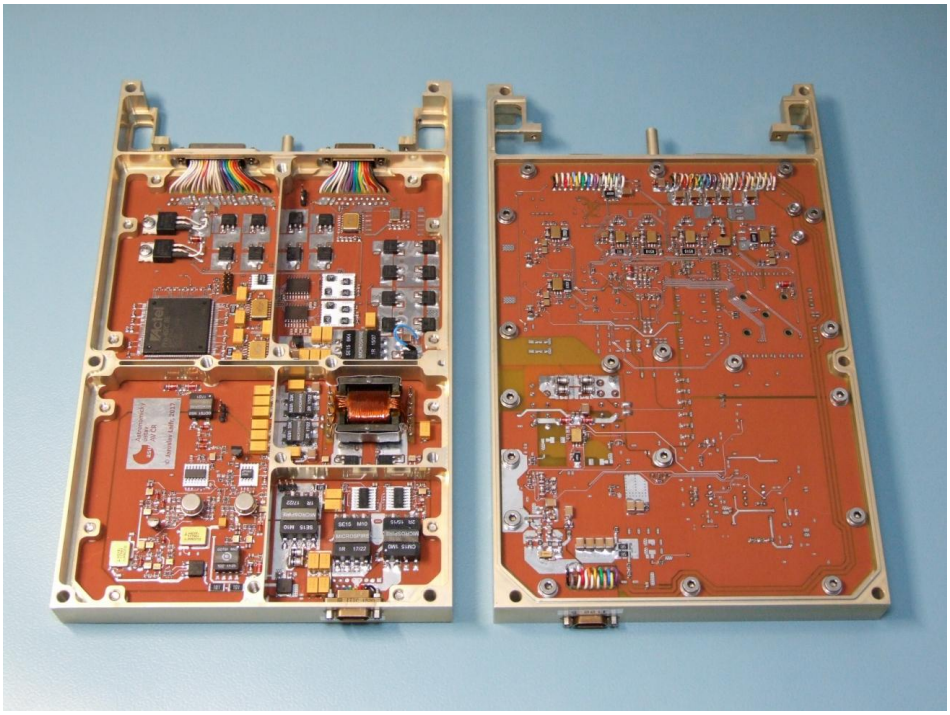

Figure 4: RPWI Low Voltage Power Supply Units assembled in Engineering Model grade.

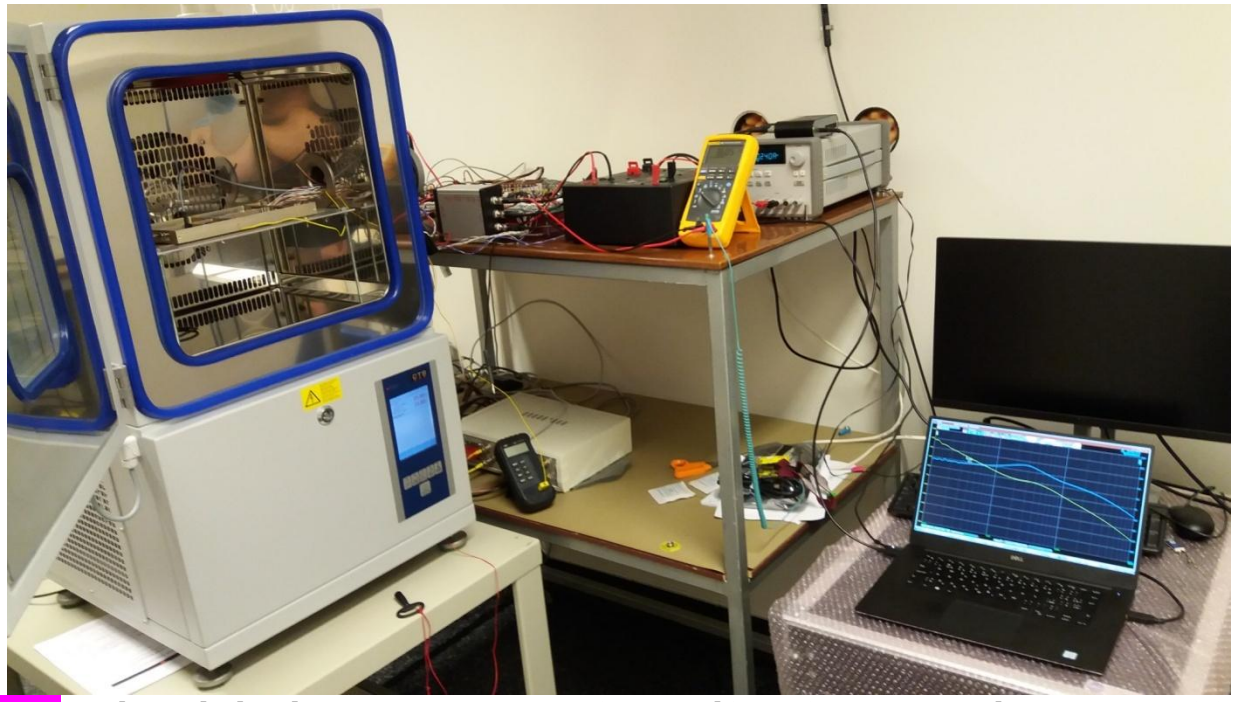

Figure 5: Thermal Chamber test setup, DUT was immersed into Nitrogen atmosphere to prevent icing.

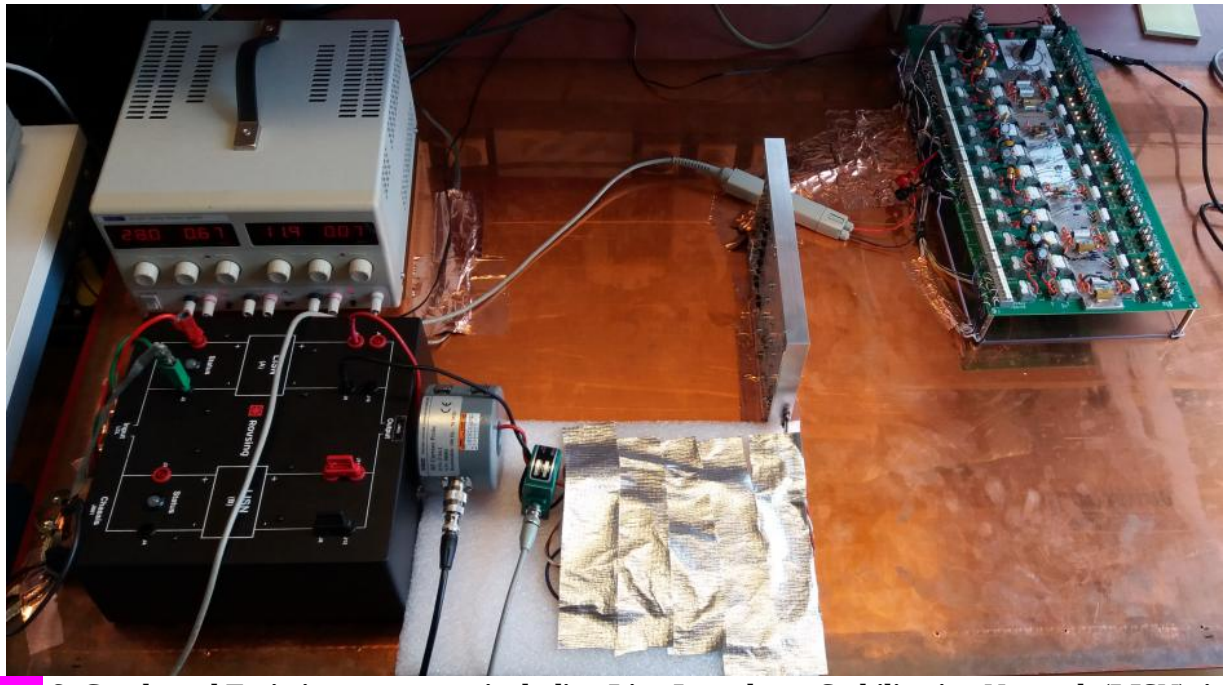

Figure 6: Conducted Emissions test setup including Line Impedance Stabilization Network (LISN), input power sensing/injection transformers and grounding of output signals.

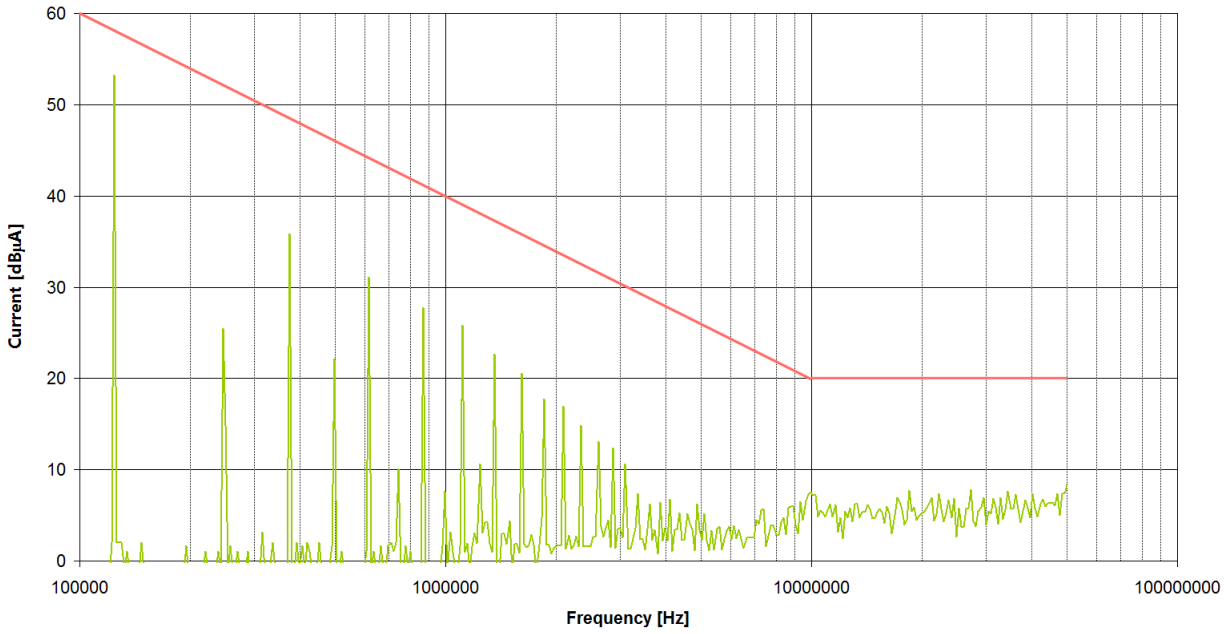

Figure 7: Differential mode emissions measured on input interface at maximum load conditions, including emission mask. Note switching frequencies are 250 / 125 kHz.

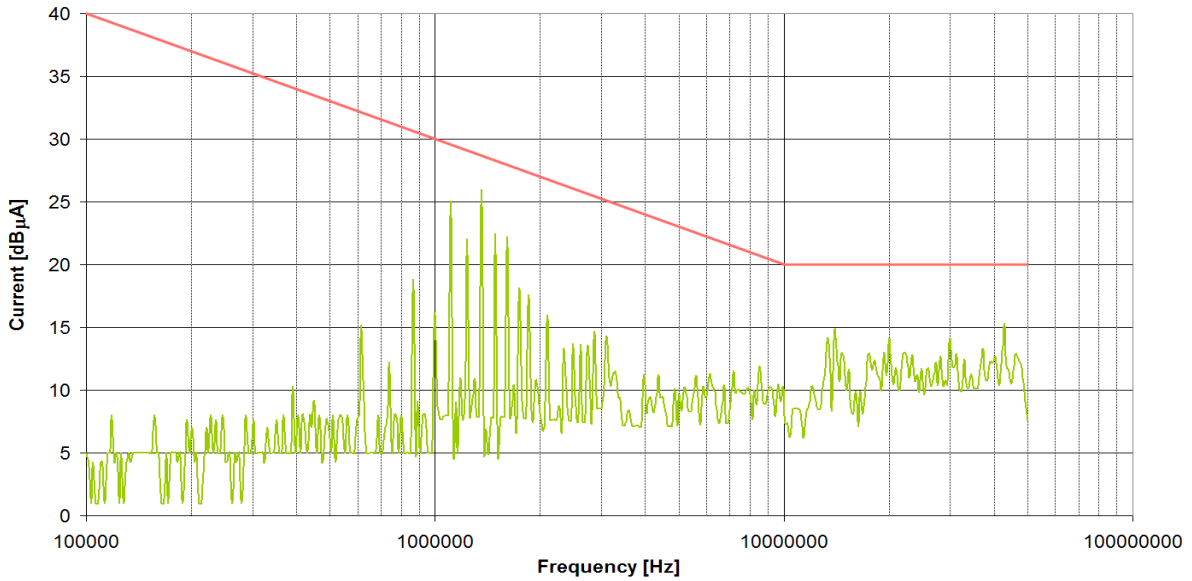

Figure 8: Common mode emissions measured on input interface at maximum load conditions. Note strict emission mask not exceeding 40 dBµA at 100 kHz. Energy of switching frequency harmonics (250 / 125 kHz) passes partially through the CM filter due to its self resonant frequency with peak at ~1.5 MHz.

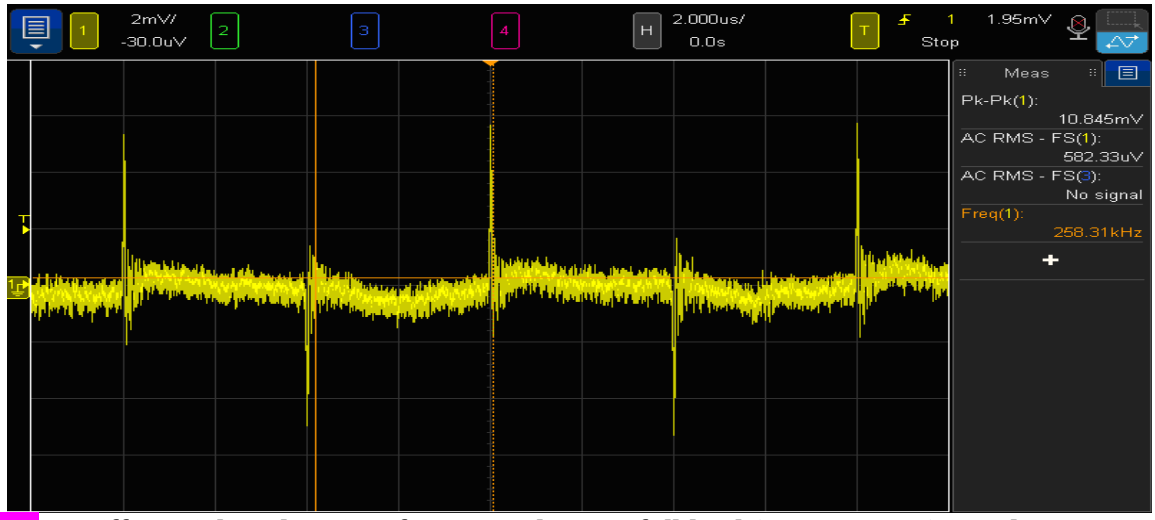

Figure 9: Differential mode noise of output voltage at full load (3.7 V @ 2.5A) is as low as 600□ V_{RMS}, with 11 mV_{pp} spikes.

Figure 10: Thermal footprint of fully loaded LVPS unit after one hour of operations under ambient air conditions. Bright (hot) spots from left to right: buck MOSFET, main power transformer and 3.7 V rail Schottky rectifiers.

10. Conclusions

Hereby presented cascaded voltage-fed push-pull DC-DC converter based on fully discrete design intended to be operated in the harsh Jovian environment aboard the ESA/JUICE mission was designed, manufactured, tested and validated. The project passed the Preliminary Design Review (PDR) in Dec, 2016 and is now closing the Critical Design Review (CDR) phase with ESA experts review. Measured high efficiency, very low noise EMC performance, implemented circuit protections, digitally controlled housekeeping readout circuits and power distribution unit together with very fast feedback loop declares that similar approach would be used on many other space missions at a fractional cost of state-of-the-art conservative solutions. Fully functional engineering models declared also very high frequency operations up to 500 / 250 kHz which further reduces input and output filtering for better scalability, where mass is a constraint. Internal timing circuits and clocking scheme allows combining the design with synchronous rectification or implementing very low voltage driving of GaN or SiC power transistors further increasing the efficiency and robustness of the converter, whilst keeping great radiation hardness. Based on the engineering model integration, verification activities and test results on the whole RPWI electronic box level, the proto flight and flight models manufacturing will follow accordingly.

11. Acknowledgement

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